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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,785	11/24/2003	John Gregory Ferrara	SIG000109	4935
34399	7590	06/15/2006	EXAMINER	
GARLICK HARRISON & MARKISON P.O. BOX 160727 AUSTIN, TX 78716-0727			PATEL, HARI	
			ART UNIT	PAPER NUMBER
			2115	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/720,785	<b>Applicant(s)</b> FERRARA, JOHN GREGORY	
	<b>Examiner</b> Hari Patel	<b>Art Unit</b> 2115	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 November 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

1. Claims 1 – 34 are presented for examination.

***Drawings***

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because:

Reference characters "**27**" (Specification), "**70**" (Fig. 1) and "**72**" (Figs. 2 and 3) have all been used to designate the RTC (real-time clock) module.

Reference characters "**70**" (Specification) and "**71**" (Fig. 3) have both been used to designate the RTC (real time clock) Digital Domain.

Reference character "**156**" has been used to designate two steps in Fig. 9. It is believed that Applicant intended for step "Overload, System Low Voltage, or Battery Low Voltage Detected?" to be designated as step **157**, according to the Specifications.

Reference character "**72**" (Specification) and "**75**" (Fig. 3) have both been used to designate the RTC (real time clock) Analog Domain.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of

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any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

**142** (Fig. 8 – “Normal Operations of IC”).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a) because they fail to show “the alarm clock interrupt module **85**” as described in the specification (paragraph [0038]. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to

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avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

5. The disclosure is objected to because of the following informalities:

Paragraph [0026] refers to Figures 15 – 17, however, no such figures are presented.

Appropriate correction is required.

***Claim Objections***

6. Claims 1, 12, 13, and 32 are objected to because of the following informalities:

7. Claim 1, line 7 and Claim 13, line 12 recite, "registers are power by a battery". It is believed that the Applicant intended for the Claims to recite, "registers are power powered by the battery".

8. Claim 12 recites, "wherein the on-chip real time clock module are located." It is recommended this be revised to recite, "wherein the on-chip real time clock module are is located".

9. Claim 32 recites "operational parameters and timing parameters ..... is stale". It is recommended that this be changed to "is are stale".

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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11. Claims 11, 13, 16, 23, 24, 29, and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 11 and 23 recite the limitation "the battery reserve" in lines 6, respectfully. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 13, lines 12-13 recite the limitation "a battery". It is unclear if this is the same battery as disclosed in Claim 13, line 7.

Also, Claim 13, lines 13-14 recite the limitation "a crystal oscillator". It is unclear if this is the same crystal oscillator as disclosed in Claim 13, line 4.

14. Claim 16, line 3 recites the limitation "an on-chip DC-to-DC converter". It is unclear if this converter is the same as the DC-to-DC converter as disclosed in Claim 13, line 5.

15. Claim 24, line 5 recites the limitation "a digital processing integrated circuit". It is unclear if this circuit is the same as the digital processing integrated circuit as disclosed in Claim 24, line 2.

16. Claim 29 recites the limitation "the plurality of persistent registers" in line 4. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 34, lines 3-4 recite the limitation "an alarm clock setting". It is unclear if this setting is the same as the alarm clock setting disclosed in Claim 33, line 3.

***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 1 – 7, 12 – 19, 24, 27 – 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Korff (U.S. Patent No. 4,573,127), and further in view of Cox (U.S. Patent No. 5,778,239), and Blau, Jr. et al. (U.S. Patent No. 4,522,333).

20. As per Claim 24, Korff teaches a digital processing circuit (*Fig. 1 – microprocessor, 20; and col. 4, lines 9-10*) comprising:

an on-chip real time clock module whose contents are periodically updated (*col. 4, lines 17-18*), wherein the contents are timing parameters (*col. 4, lines 48-61*);

a processor (*Fig. 1 – CPU, 22*) that periodically updates the contents of the real time clock module (*col. 4, lines 48-50 and 61-64*).

21. Korff does not specifically teach that the contents of the real time clock module are operational parameters being managed, and wherein the real time clock module is powered by a power source and receives a clock signal from a crystal oscillator that remain active when the digital processing system is powered down. Korff also does not teach that the real time clock module provides the digital processing integrated circuit with the parameters when parameters of the integrated circuit are "stale". Specifically, Korff teaches a real time clock module whose contents are periodically updated. Korff fails specifically to teach that the stored contents are operational parameters, management of the parameters when they are found to be stale, and the power and signal sources for the real time clock module.

22. Cox teaches a real time clock module (*Fig. 1*), wherein operational ("setup") parameters are stored in the real time clock module (*col. 2, lines 16-19*).

23. It would have been obvious to one of ordinary skill in the art to combine the teachings of Korff and Cox because they both teach a real time clock module capable of storing contents. Cox's teaching of system parameters stored in the real time clock module shows the type of contents that may be stored in a real time clock module.

24. Blau, Jr. et al. (hereinafter, referred to as "Blau") teach a circuit comprising a real time clock module, wherein a crystal oscillator maintains a clock signal to the real time

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clock module and a battery maintains power supplied to the real time clock module when a power failure occurs (*col. 4, lines 67-68, col. 5, lines 1-7 and; Fig. 2*).

Blau also discloses that the battery allows the processor to resume operation when main power is reestablished using retained information stored before a power-off (*col. 5, lines 2-7*).

25. It would have been obvious to one of ordinary skill in the art to combine the teachings of Korff and Blau because they both teach a real time clock module, both inherently needing a power source and clock signal to operate. Blau's teaching of the disclosed crystal oscillator and battery show that the real time clock module can maintain its functionality when power to the system is not available. In reference to the applicant's claimed method, it would have obvious that Blau's teachings can be applied to a real time clock module located on an integrated circuit, wherein power and a crystal oscillator signal are maintained at the real time clock module when power is not being supplied to the rest of the integrated circuit. Inherently, the contents ("information") stored in the real time clock module would be provided to the processor or the digital processing integrated chip comprising the real time clock module. During a power-off state, information contents stored in the digital processing integrated circuit are inherently "stale" compared to the retained information backed up in the storage of the real time clock module, thus it would be required that the real time clock module provide the retained information content to the digital processing integrated circuit after the integrated circuit has resumed power-on. It is also well known in the art that audio

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processing chips may contain a digital processing integrated circuit comprising a real time clock module.

26. As per Claim 27, Cox teaches a method of monitoring battery power levels (*col. 2, lines 32-42*). It is well known in the art that a digital processing integrated circuit would power down when battery levels go below a predetermined threshold and that current parameters would be stored prior to the power down, wherein the parameters could be stored on the real time clock module.

27. As per Claim 28, since Blau teaches that the crystal oscillator only maintains a clock signal to the real time clock module (*Fig. 2 and; col. 4, lines 67-68*), the rest of the digital processing integrated circuit would inherently operate on another clock domain, or the system clock domain.

28. As per Claim 29, it is well known in the art that when two clock domains are being used within an integrated circuit, wherein communication occurs between the two domains (in this instance, between the digital processing integrated circuit and the real time clock module), it would have been obvious to use a module/circuit to synchronize the two domains so that data can be synchronously transferred between the two domains.

29. As per Claim 30, since the digital processing integrated circuit comprises two clock domains, it would have been obvious to one of ordinary skill in the art to use input/output buffers to temporarily store the parameters that are transferred from one clock domain to another since buffers are used to compensate for differences in operating speeds.

30. As per Claim 31, as mentioned above, Blau teaches that the real time clock module maintains a powered state when the rest of the system is powered down (*col. 4, lines 67-68, col. 5, lines 1-7*).

31. As per Claims 1, 3, 5, 6, 7, 12 it is directed to an apparatus of the on-chip real time clock module/digital processing integrated circuit method as set forth in Claims 24 and 27 – 31 above. Since Korff–Cox–Blau teach the claimed method of managing parameters of a digital processing integrated circuit comprising an on-chip real time clock module, Korff–Cox–Blau also teach the apparatus having a digital processing integrated circuit and real time clock module.

32. As per Claim 2, since the digital processing integrated circuit operates on a different clock domain than of the on-chip real time clock module, and since parameters are transferred between the two domains, an interface is inherently required between the real time clock module and integrated circuit to exchange the information.

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33. As per Claim 4, it would have been obvious to one of ordinary skill in the art that an on-chip DC-to-DC converter powers the digital processing integrated circuit since, typically, integrated circuits use DC-to-DC converters with the circuit comprises a battery.

34. As per Claims 13 – 19, Korff–Cox–Blau teach the claimed digital processing integrated circuit as applied to Claims 1 – 7 above.

35. Claims 8 – 11, 20 – 23, 25, 26, 32 – 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Korff, Cox, and Blau, Jr. et al. as applied to Claim 24 above, and further in view of Cornish et al. (U.S. Patent No. 5,943,507).

36. As per Claim 25, Korff–Cox–Blau teach the method of Claim 24 as mentioned above, however they do not teach that the digital processing integrated circuit comprises shadow registers to store the parameters. Specifically, Korff–Cox–Blau teach that the parameters are stored in an on-chip real time clock module and are provided to the digital processing integrated circuit. Korff–Cox–Blau fail to teach where the parameters are stored within the digital processing integrated circuit.

37. Cornish et al. (hereinafter, referred to as “Cornish”) discloses a digital processing integrated circuit (*Fig. 11 – PPU 110 and; col. 15, lines 47-48*) comprising:

an on-chip real time clock module (*Fig. 11 – RTC, 918 and col. 16, lines 29-31*)  
and;  
shadow registers (*col. 17, lines 18-19*).

38. It would have been obvious to one of ordinary skill in the art to combine the teachings of Korff–Cox–Blau and Cornish because they all teach the use of a real time clock module. Cornish's teaching of shadow registers comprised within the digital processing integrated circuit would allow a storage means for parameters temporarily stored in the real time clock module to be transferred to when power is restored in the digital processing integrated circuit.

39. As per Claim 26, it would have been obvious to one of ordinary skill in the art that the parameters contained within the shadow registers return to a default condition when the digital processing integrated circuit is powered down so that stale parameters can be detected after a power-down of the digital processing integrated circuit.

40. As per Claim 32, after parameters return to a default condition in response to a power-down of the digital processing integrated circuit, it is inherent that those parameters stored in the integrated circuit are stale from that point on, including at a state of power-up since the parameters cannot be updated while power is not being supplied to the integrated circuit in a powered-down state.

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41. As per Claims 33 and 34, to power up the digital processing integrated circuit, inherently, an interrupt signal would need to be issued to the digital processing integrated circuit. It is known in the art that powering up a circuit may require a method of issuing a power-on interrupt/signal to the circuit in response to an alarm clock setting.

The real time clock module provides the digital processing integrated circuit with current parameters when parameters of the digital processing integrated circuit are found to be stale, as applied to Claim 24 above. The parameters are found to be stale at a state of power-up, as applied to Claim 32 above, thus, the real time clock module would supply current parameters to the digital processing integrated circuit at power up.

42. As per Claims 8 – 11, it is directed to an apparatus of the on-chip real time clock module/digital processing integrated circuit method as set forth in Claims 25, 26, 32 – 34 above. Since Korff–Cox–Blau teach the claimed method of managing parameters of a digital processing integrated circuit comprising an on-chip real time clock module, Korff–Cox–Blau also teach the apparatus having a digital processing integrated circuit and real time clock module.

43. As per Claims 20 – 23, Korff–Cox–Blau teach the claimed digital processing integrated circuit as applied to Claims 8 – 11 above.

**Conclusion**

44. Any inquiry concerning this communication from the examiner should be directed to Hari Patel whose telephone number is 571-272-2743. The examiner can normally be reached on Monday – Thursday from 8:00am – 5:30pm and every other Friday from 8:00am – 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee, can be reached at 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of the application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Hari Patel  
Examiner  
Art Unit 2115

  
**CHUN CAO**  
**PRIMARY EXAMINER**